Amendments to the Specification

Please replace the paragraph found on page 7, lines 10 – 18 with the following amended paragraph:

The reference clock is received by each channel card clock module ~~42~~ 40, and synthesized according to the direct-digital-synthesis technique more fully described in U.S. Patent Number 6,188,253. Generally, though, the reference clock signal increments a 48-bit accumulator, which then feeds a phase-locked-loop to generate a sinusoidal re-creation of the reference clock. Divider circuitry (not shown) divides the frequency of the signal to create varying clocks for the different ASICs, including the master oscillator clock signal of between 1 to 2 gigahertz. The filtering circuitry 44 formats the clock waveform to make it more suitable for the pattern generation/timing clock inputs.